#### 10085919 CLS

Most Frequently Occurring Classifications of Patents Returned From A Search of 10085919 on June 15, 2004

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Original Classifications
  14 714/726
   5
      714/727
      714/729
   3
     714/731
   2
     324/158.1
   2 324/73.1
   2
     327/199
   2
      327/202
   2
      714/728
      714/733
 Cross-Reference Classifications
     714/733
   8
     714/726
      324/73.1
   5
     714/729
   4
      714/724
      714/727
   4
      714/731
   3
      714/736
   2
     324/158.1
   2 327/291
   2
     327/299
   2
     365/201
   2
     712/220
   2
     714/730
   2
      714/732
   2
      714/734
      714/739
 Combined Classifications
      714/726
  22
\bigcirc 11
      714/733
  10
      714/729
      714/727
   9
      324/73.1
   7
      714/731
   5
      714/724
      324/158.1
   3
      714/732
   3
      714/736
   2
      327/199
      327/202
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2	327/291
2	327/299
2	365/201
2	712/220
2	714/728
2	714/730
2	714/734
2	714/738
2	714/739

### 10085919 CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returne

From A Search of 10085919 on June 15, 2004

22	714/726 Class 714/699 714/724 714/726	14: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING	sca
n		design (LSSD))	
11	714/733 Class	(2 OR, 9 XR)  14: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY	
	714/699 714/724 714/733	PULSE OR DATA ERROR HANDLING .Digital logic testing	
10	714/729 Class	(5 OR, 5 XR)  14: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY	
	714/699 714/724 714/726	PULSE OR DATA ERROR HANDLING	sca
n	714/729	design (LSSD))Plural scan paths	
9	714/727 Class 714/699 714/724 714/726	14: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING	sca
n	714/727	design (LSSD))Boundary scan	
7		(2 OR, 5 XR) 24 : ELECTRICITY: MEASURING AND TESTING PLURAL, AUTOMATICALLY SEQUENTIAL TESTS	
7	714/731 Class	(3 OR, 4 XR)  14: ERROR DETECTION/CORRECTION AND FAULT	

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DETECTION/RECOVERY

n	714/699 714/724 714/726	10085919_CLSTITLES PULSE OR DATA ERROR HANDLING .Digital logic testingScan path testing (e.g., level sensitive sca		
11	714/731	<pre>design (LSSD))Clock or synchronization</pre>		
į	714/699	: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING		
	714/724	.Digital logic testing		
2		OR, 2 XR) : ELECTRICITY: MEASURING AND TESTING MISCELLANEOUS		
3	3 714/732 (1 Class 714	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY		
	714/699 714/724 714/732	PULSE OR DATA ERROR HANDLING .Digital logic testingSignature analysis		
3	3 714/736 (0 Class 714	OR, 3 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY		
	714/699 714/724 714/736			
2		OR, 0 XR) : MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS		
	327/100 327/185	SIGNAL CONVERTING, SHAPING, OR GENERATING .Particular stable state circuit (e.g.,		
	327/199	<pre>tristable, etc.)Circuit having only two stable states (i.e.,   bistable)</pre>		
2		OR, 0 XR) : MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS		
	327/100	SIGNAL CONVERTING, SHAPING, OR GENERATING .Particular stable state circuit (e.g.,		
	327/185	tristable, etc.)		

# 10085919\_CLSTITLES bistable)

...Master-slave bistable latch 327/202

n

714/726

	3277202		Master stave bistable laten
2 327/291 Class		327	: MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS
	327/100 327/291		SIGNAL CONVERTING, SHAPING, OR GENERATING .Clock or pulse waveform generating
2	327/299 Class		OR, 2 XR) : MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS
	327/100 327/291 327/299		SIGNAL CONVERTING, SHAPING, OR GENERATING .Clock or pulse waveform generatingSingle clock output with single clock input or data input
2		365 .01	: STATIC INFORMATION STORAGE AND RETRIEVAL READ/WRITE CIRCUIT
2	712/220 Class		OR, 2 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INS
TRUC	TION		
	712/220		PROCESSING CONTROL
2	· · · · · · · · · · · · · · · · · · ·		OR, 0 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/699		PULSE OR DATA ERROR HANDLING
	714/724		.Digital logic testing
<b>n</b>	714/726		Scan path testing (e.g., level sensitive sca
n			design (LSSD))
	714/728		Random pattern generation (includes pseudorandom pattern)
2	714/730 Class	(0 714	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/699 714/724		PULSE OR DATA ERROR HANDLING .Digital logic testing

design (LSSD))

..Scan path testing (e.g., level sensitive sca

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714/730	$\dots$ Address $\overline{i}$ ng

2	714/734 Class 714/699 714/724 714/734	714	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT     DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingStructural (in-circuit test)
2	714/738 Class 714/699 714/724 714/738	•	OR, 1 XR) : ERROR DETECTION/CORRECTION AND FAULT     DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingIncluding test pattern generator
2	714/739 Class 714/699 714/724 714/738 714/739		OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT     DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingIncluding test pattern generatorRandom pattern generation (includes pseudorandom pattern)

PLUS Search Results for S/N 10085919, Searched June 15, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear ch

system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that a re

most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

## 10085919\_LIST

5396170
5504756
5838693
5881067
5886901
6016564
6289477
6256770
6308291
6370664
6380724
6389567
6393592
6463561
6573703

## 10085919\_QUAL

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53 53 55 58 58 60 62 63 63 63	23 96 04 38 81 86	40 17 75 69 06 90 54 77 29 66 72 56	0 0 6 3 7 1 4 7 0 1 4 4 7	66 66 66 66

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